EAST - [10614892.wsp 1]

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  - L1: (98) (corner near (trench adj isolation)
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DBs | USPAT; EPO; JPO; DERWENT; IBM_TDB | Plurals

Default operator: OR | Highlight all hit terms initially

1 and spacer$1

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	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6670279 B1	20031230	22	Method of forming shallow trench isolation with rounded corners and divot-free by	438/719	216/39; 216/79;
2	☐	☐	US 6573556 B2	20030603	29	Parasitic surface transfer transistor cell (PASTT cell) for bi-level and multi-level	257/315	257/366; 257/386
3	☐	☐	US 6555442 B1	20030429	16	Method of forming shallow trench isolation with rounded corner and divot-free by	438/424	257/E21.55
4	☐	☐	US 6483148 B2	20021119	10	Self-aligned elevated transistor	257/347	257/278; 257/288;
5	☐	☐	US 6440817 B2	20020827	15	Methods of forming integrated circuitry	438/424	257/E21.507; 257/E21.549;
6	☐	☐	US 6429081 B1	20020806	29	Parasitic surface transfer transistor cell (PASTT cell) for bi-level and multi-level	438/301	438/257
7	☐	☐	US 6399977 B1	20020604	20	Reducing oxidation stress in the fabrication of devices	257/301	257/303; 257/E21.651;
8	☐	☐	US 6355540 B2	20020312	8	Stress-free shallow trench isolation	438/433	257/510; 257/E21.549;
9	☐	☐	US 6348389 B1	20020219	7	Method of forming and etching a resist protect oxide layer including end-point etch	438/305	257/E21.252; 438/586;
10	☐	☐	US 6326272 B1	20011204	10	Method for forming self-aligned elevated transistor	438/300	257/E21.206; 257/E21.426;
11	☐	☐	US 6319794 B1	20011120	19	Structure and method for producing low leakage isolation devices	438/424	257/E21.549; 438/427;

HTML

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